

**Amendments to the Specification (other than claims):**

Please replace paragraph [0046] with the following amended paragraph:

[0046] Fig. 5B shows the relationship between the windows and the micro-apertures that are formed in the mask layer, and is a cross section taken in the [[VI-B]] IV-B direction in Fig. 5A.

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Please replace paragraph [0070] with the following amended paragraph:

*34*  
[0070] As illustrated in Fig. 1, the method of manufacturing a Group III nitride semiconductor crystal of this mode of embodiment allows the area of the principal face of the Group III semiconductor crystal (this corresponds to ~~the lower surface 10~~ the lower surface 10a or the upper surface 10b in Fig. 1) to be made smaller than the area of the principal face 1h of the starting substrate 1. It is therefore possible to directly and efficiently manufacture a Group III nitride semiconductor crystal about the size of a semiconductor device even when a large starting substrate is used.

Please replace paragraph [0085] with the following amended paragraph:

[0085] The rate at which the Group III nitride semiconductor crystal of this mode of embodiment is grown preferably is at least [[10  $\mu\text{m}$ ]] 10  $\mu\text{m}/\text{hr}$  but not more than [[300  $\mu\text{m}$ ]] 300  $\mu\text{m}/\text{hr}$ . A Group III nitride semiconductor crystal growth rate that is less than [[10  $\mu\text{m}$ ]] 10  $\mu\text{m}/\text{hr}$  will lower manufacturing efficiency, whereas if it

exceeds [[300  $\mu\text{m}$ ]] 300  $\mu\text{m}/\text{hr}$ , defects such as holes are likely to be introduced into the Group III nitride semiconductor crystal and make it more prone to cleaving.

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Please replace paragraph [0116] with the following amended paragraph:

[0119] The rate at which the Group III nitride semiconductor crystal substrate of this mode of embodiment is grown preferably allows growth of a Group III nitride semiconductor crystal substrate that is at least [[10  $\mu\text{m}$ ]] 10  $\mu\text{m}/\text{hr}$  but not more than [[300  $\mu\text{m}$ ]] 300  $\mu\text{m}/\text{hr}$ . A rate of growth that produces a Group III nitride semiconductor crystal substrate that is less than [[10  $\mu\text{m}$ ]] 10  $\mu\text{m}/\text{hr}$  will lower manufacturing efficiency, whereas when this is greater than [[300  $\mu\text{m}$ ]] 300  $\mu\text{m}/\text{hr}$ , defects such as holes easily occur in the Group III nitride semiconductor crystal substrate and make it more prone to cleaving.

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Please replace paragraph [0131] with the following amended paragraph:

[0131] As illustrated in Fig. 5, the windows 2a of the mask layer 2 is made of a group of at least two micro-apertures [[2b]] 2s. There are no particular limitations regarding the arrangement of the micro-apertures [[2b]] 2s, however, from the perspective of growing a uniform Group III nitride semiconductor crystal, preferably they are arranged uniformly at a constant spacing in such a manner that the center of the micro-apertures is the apex of an equilateral triangle or a regular square. The width  $W_s$  of the micro-apertures preferably is at least 0.5  $\mu\text{m}$  but not more than 200  $\mu\text{m}$ , and the pitch  $P_s$  between micro-apertures preferably is at least 1  $\mu\text{m}$  but not more

than 250  $\mu\text{m}$ . When the width  $W_s$  of the micro-apertures is less than 0.5  $\mu\text{m}$ , inexpensive photolithography cannot be used and this increases the manufacturing costs, whereas when over 200  $\mu\text{m}$ , the effect of inhibiting cleaving in the Group III nitride semiconductor crystal substrate is reduced. When the pitch  $P_s$  of the micro-apertures is less than 1  $\mu\text{m}$ , inexpensive photolithography cannot be used and this increases the manufacturing costs, whereas when over 250  $\mu\text{m}$ , the effect of inhibiting cleaving in the Group III nitride semiconductor crystal substrate is reduced.

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*99*  
Please replace paragraph [0135] with the following amended paragraph:

*99*  
[0135] Next, the Group III nitride semiconductor crystal 10, which is constituted by the Group III nitride semiconductor crystal substrate 11 and the Group III nitride semiconductor crystal layer 12, is separated from the starting substrate 1 like in Embodiment Mode 5 as shown in Fig. 6C. In this mode of embodiment, if the seed crystal [[2]] 4 has been placed on the starting substrate 1 as in Embodiment Mode 5a (Embodiment Mode 10a), then the Group III nitride semiconductor crystal 10 grown from the seed crystal 4 does not adhere tightly to the starting substrate 1 and thus the Group III nitride semiconductor crystal 10 can be separated from the starting substrate 1 simply by applying a small force.

*104*  
Please replace paragraph [0142] with the following amended paragraph:

*104*  
[0142] As shown in Fig. 9, the semiconductor device more specifically is a Group III nitride semiconductor device 90 that functions as an LED, in which an n-type GaN layer serving as an n-type Group III nitride semiconductor crystal layer 21, an

$\text{In}_{0.2}\text{Ga}_{0.8}\text{N}$  layer 22a and an  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  layer 22b serving as a light-emitting layer 22, and a p-type GaN layer serving as a p-type Group III nitride semiconductor crystal layer 23 are grown in that order atop the Group III nitride semiconductor crystal substrate 11 as the one or more Group III nitride semiconductor crystal layers 12, and also an n-side electrode 51 is formed on the lower surface of the Group III nitride semiconductor crystal 10 (this corresponds to the lower surface of the Group III nitride semiconductor crystal substrate 11) and a p-side electrode 52 is formed on the upper surface of the Group III nitride semiconductor crystal 10 (this corresponds to the upper surface of the p-type nitride semiconductor crystal layer 23), and this Group III nitride semiconductor device 90 emits emission rays 98. It should be noted that the light-emitting layer 22 also can have a MQW (Multi-Quantum Well) structure that is achieved by layering multiple units of a two-layered structure composed of a GaN layer and an  $\text{In}_{0.2}\text{Ga}_{0.8}\text{N}$  layer.

Please replace paragraph [0152] with the following amended paragraph:

[119]  
[0152] In the light-emitting appliance of this mode of embodiment, it is preferable that the GaN substrate, which is a Group III nitride crystal substrate, is provided with n-type character by doping with Si (silicon) and/or O (oxygen), that the O atom density is in the range of  $1 \times 10^{17} \text{ cm}^{-3}$  to  $5 \times 10^{19} \text{ cm}^{-3}$ , and that the GaN substrate is at least  $100 \mu\text{m}$  but not more than  $600 \mu\text{m}$  thick. The Si atom and/or O atom density of the substrate significantly impacts the resistivity and the light transmittance of the substrate, and the thickness of a substrate significantly affects its light transmittance.

An Si atom and/or O atom density less than  $1 \times 10^{17} \text{ cm}^{-3}$  results in a large light transmittance but also results in a large resistivity, whereas when this is over  $5 \times 10^{19} \text{ cm}^{-3}$  the resistivity becomes small but the light transmittance also becomes small, and in both cases the end result is a drop in light-emission efficiency. When the substrate is less than [[10]] 100  $\mu\text{m}$  thick there is a drop in its mechanical strength, whereas a substrate thickness over 600  $\mu\text{m}$  will result in a drop in light transmittance and lower the light-emission efficiency.

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10,598,173* Please replace paragraph [0210] with the following amended paragraph:

*173  
[0210] Implementation 39*

In this implementation, the same method as that of Implementation 1 was used to form a 50 nm thick  $\text{SiO}_2$  layer as a mask layer on a 5.08 cm diameter  $\times$  400  $\mu\text{m}$  thick sapphire substrate serving as the starting substrate 1 and then provide windows 2a each made from a group of at least two or more micro-apertures [[2b]]  
2s, as illustrated in Fig. 4, which corresponds to Embodiment 9. Here, the window pitch  $P_w$  was 2200  $\mu\text{m}$ , the aperture width  $W_w$  was 2000  $\mu\text{m}$ , the micro-aperture pitch  $P_s$  was 2  $\mu\text{m}$ , and the micro-aperture width  $W_s$  was 1  $\mu\text{m}$ . Next, a GaN substrate was grown as the Group III nitride semiconductor crystal substrate 11 on the open surface 1a of the sapphire substrate through HVPE under the conditions shown in Table XII without allowing cleaving to occur. Then, as in Implementation 1, MOCVD was employed to grow a 5  $\mu\text{m}$  thick n-type GaN layer serving as the n-type Group III nitride semiconductor crystal layer 21, a 3 nm thick  $\text{In}_{0.2}\text{Ga}_{0.8}\text{N}$  layer 22a

and a 60 nm thick  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  layer 22b serving as the light-emitting layer 22, and a 150 nm p-type GaN layer serving as the p-type Group III nitride semiconductor crystal layer 23, in that order, on the GaN substrate as the one or more Group III nitride semiconductor crystal layers 12. Next, as in Implementation 1, a p-side electrode was formed, the Group III nitride semiconductor crystal and the starting substrate were separated, and an n-side electrode was formed, producing an LED. The relative strength of the emission spectrum of this LED at the peak wavelength 450 nm was assessed. The results are shown in Table XII.

Please replace paragraph [0216] with the following amended paragraph:

A 400  $\mu\text{m}$  thick GaN substrate was obtained as the Group III nitride semiconductor crystal substrate 11 in the same manner as the first through 14<sup>th</sup> process steps of Comparative Example 1, as illustrated by Figs. 14A and 14C, except that the raw gas flow rate, the crystal growth temperature, and the crystal growth time were those shown in Table XIV. Next, as shown in Fig. 10, a 3  $\mu\text{m}$  thick i-type GaN layer 12a and a 30 nm thick i-type Al<sub>0.25</sub>[[Ga<sub>0.85</sub>]] Ga<sub>0.75</sub>N layer 12b were grown on the GaN substrate through MOCVD as the one or more Group III nitride [[semiconductor crystal layers 12 (15th Step).]]

Please replace paragraph [0217] with the following amended paragraph:

[0217] As illustrated in Fig. 10, photolithography and lift-off ensued to form a source electrode 53 and a drain electrode 55 on the i-type  $\text{Al}_{0.25}[(\text{Ga}_{0.85})]\text{Ga}_{0.75}\text{N}$  layer 12b

by heating compound layers each made of a Ti layer (50 nm thick) / Al layer (100 nm thick) / Ti layer (20 nm thick) / Au layer (200 nm thick) for 30 seconds at 800°C to produce alloys thereof (16<sup>th</sup> process). A 300 nm thick Au layer was then formed as a gate electrode 54 (17<sup>th</sup> process). The gate length was 2  $\mu\text{m}$  and the gate width was 150  $\mu\text{m}$ . The Group III nitride semiconductor crystal made of the Group III nitride semiconductor crystal substrate and the Group III nitride semiconductor crystal layer was then separated into 400  $\mu\text{m} \times$  400  $\mu\text{m}$  chips (18<sup>th</sup> process), producing HEMT semiconductor devices 100.

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Please replace paragraph [0219] with the following amended paragraph:

*200*  
[0219] Next, as shown in Fig. 2B, a crystal was grown through HVPE under the conditions of GaCl gas flow rate 110 sccm, NH<sub>3</sub> gas flow rate 6000 sccm, growth temperature 1050°C, and growth time one hour (3rd Step), yielding a 300  $\mu\text{m} \times$  300  $\mu\text{m} \times$  85  $\mu\text{m}$  thick GaN substrate as a Group III nitride semiconductor crystal substrate 11 on the open surface 1a of the starting substrate 1 located below the windows 2a of the mask layer 2 and on some of the upper surface 2b of the mask layer surrounding the windows 2a. Then, as illustrated in Fig. 10, a 3  $\mu\text{m}$  thick i-type GaN layer 12a and a 30 nm thick i-type Al<sub>0.25</sub>[[Ga<sub>0.85</sub>]] Ga<sub>0.75</sub>N layer 12b were grown on the Group III nitride semiconductor crystal substrate 11 through MOCVD as the one or more Group III nitride semiconductor crystal layers 12 (4th Step).

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Please replace paragraph [0220] with the following amended paragraph:

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[0220] Next, as illustrated in Fig. 10, photolithography and lift-off ensued to form a source electrode 53 and a drain electrode 55 on the i-type  $\text{Al}_{0.25}[\text{Ga}_{0.85}]$  Ga<sub>0.75</sub>N layer 12b by heating compound layers each made of a Ti layer (50 nm thick) / Al layer (100 nm thick) / Ti layer (20 nm thick) / Au layer (200 nm thick) for 30 seconds at 800°C to produce alloys (5th Step). A 300 nm thick Au layer was then formed as a gate electrode 54 (6th Step). The gate length was 2  $\mu\text{m}$  and the gate width was 150  $\mu\text{m}$ . Next, as illustrated by Fig. 2C, this was soaked in aqueous hydrofluoric acid (hydrofluoric acid: 1 wt%) to etch away the mask layer 2 (7th Step), after which, as shown in Fig. 2D, it was soaked in aqueous KOH (KOH: 5 wt%) to etch the lower surface 10a (atomic layer made of elemental nitrogen) of the Group III nitride semiconductor crystal 10 that is in contact with the starting substrate 1 to separate the Group III nitride semiconductor crystal 10 and the starting substrate 1 (8th Step), producing a HEMT semiconductor device 100.

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Please replace paragraph [0249] with the following amended paragraph:

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[0249] Next, as illustrated in Fig. 13, the element was mounted so that its p-type GaN layer 23b-side is in contact with the mount portion [[a]] 60a of the lead frame, forming a light-emitting appliance. The conductive resin 62 applied to the mount portion fastens the element and the mount to one another and allows electrical conductivity.